Subt A'

What is claimed is:

1. A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a bottom portion and substantially vertical sidewalls;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls;

a gate electrode overlying the gate dielectric layer; and

source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals have an extension which extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess.

Subt C2

2. The transistor of Claim 1, further comprising a portion of the gate electrode that overlies an innermost portion of the source/drain extension:

3. The structure of Claim 2, wherein the gate electrode conforms to the recessed channel.

Subt A2

4. A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having bottom portion and tapered sidewalls, the tapered sidewall surfaces forming an obtuse angle with respect to the bottom portions of the recess;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the tapered sidewalls;

a gate electrode overlying the gate dielectric layer; and

source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals have an extension which extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess.

Subt C4

5. The transistor of Claim 4, wherein a portion of the gate electrode that overlies an innermost portion of the source/drain extension.

6. The transistor of Claim 4, wherein the gate electrode conforms to the recessed channel.

Subt a3

7. A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a curvilinear shape;

a gate dielectric layer disposed superjacent the curvilinear recess;

a gate electrode overlying the gate dielectric layer; and

source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals have an extension which extends downwardly, from approximately the surface of the substrate, along the curvilinear sides of the recess.

Subt C6

8. The transistor of Claim 6, wherein a portion of the gate electrode that overlies an innermost portion of the source/drain extension.

9. The transistor of Claim 6, wherein the gate electrode conforms to the recessed channel.

10. A method of making a microelectronic device, comprising:

forming a first layer over a substrate;

forming openings in the first layer, the openings exposing a portion of the substrate, the openings having substantially vertical sidewalls;

forming a first spacer adjacent the sidewalls of the first layer openings;

forming a second spacer adjacent the first spacer;

etching a portion of the exposed substrate;

removing the second spacer;

forming a dielectric layer superjacent the exposed portions of the substrate;

forming an electrode superjacent the dielectric layer; and

removing the first layer.

11. The method of Claim 10, wherein etching a portion of the exposed substrate comprises isotropically etching the substrate.

12. The method of Claim 10, wherein etching a portion of the exposed substrate comprises anisotropically etching the substrate.

13. The method of Claim 10, further comprising oxidizing the exposed portions of the substrate, and wherein the etching a portion of the exposed substrate comprises etching the oxidized portions of the substrate.

14. A method of forming a field effect transistor, comprising:

depositing an etch stop layer and a damascene layer over a silicon substrate;

removing portions of the damascene and etch stop layers to expose portions of the silicon, and form sidewalls in the damascene and etch stop layers;

forming a first spacer layer along the sidewalls of the damascene layer and the etch stop layer;

etching the exposed silicon;

removing the second spacer; forming a gate dielectric layer superjacent the etched silicon; and depositing a gate electrode layer over the damascene and gate dielectric layers;

planarizing the gate electrode layer so as to form a gate electrode;

removing the damascene, second spacer, and etch stop layers; and

forming source/drain terminals self-aligned to the gate electrode.

15. The method of Claim 14, wherein planarizing the gate electrode layer comprises chemical mechanical polishing using the damascene layer as a polish stop.

16. The method of Claim 14, further comprising implanting ions into the silicon substrate.

17. The method of Claim 14, further comprising implanting ions into the silicon substrate, after the first and second spacers are formed.

18. The method of Claim 14, further comprising performing a channel implant into the silicon using the damascene, first spacer, and second spacer layers as implant masks.

19. The method of Claim 14 wherein forming source/drain terminals comprises implanting ions of a first conductivity type into the silicon, adjacent to the gate electrode; forming third spacers adjacent to the gate electrode, and implanting ions of a first conductivity type into the silicon, adjacent to the third spacers.

20. The method of Claim 14, wherein etching the silicon comprises an anisotropic etch.

21. The method of Claim 14, wherein etching the silicon comprises an isotropic etch.

22. A method of forming a field effect transistor, comprising:

depositing an etch stop layer and a damascene layer over a silicon substrate;

removing portions of the damascene and etch stop layers to expose portions of the silicon, and form sidewalls in the damascene and etch stop layers;

forming a first spacer layer along the sidewalls of the damascene layer and the etch stop layer, and a second spacer adjacent the first spacer layer;

oxidizing the exposed silicon;

etching the exposed oxidized silicon;

removing the second spacer; forming a gate dielectric layer superjacent the etched silicon; and depositing a gate electrode layer over the damascene and gate dielectric layers;

planarizing the gate electrode layer so as to form a gate electrode;

removing the damascene, second spacer, and etch stop layers; and

forming source/drain terminals self-aligned to the gate electrode.